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# JOINT SERVICES ELECTRONICS PROGRAM

**FINAL REPORT**  
(Contract F49620-90-C-0029)  
6 June 1990 - June 5, 1993)

*Jeffrey Bokor and Michael A. Lieberman*

31 July 1993

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**ELECTRONICS RESEARCH LABORATORY**  
College of Engineering  
University of California, Berkeley, CA 94720

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13. ABSTRACT (Maximum 200 words)  This report summarizes the research activity supported by the Joint Services Electronics Program at the Electronics Research Laboratory for the period June 1990 to June 1993. It includes the Director's overview, a listing of principal investigators, degrees awarded to students and a list of publications and presentations. The research was organized into three themes during this period: Quantum Electronic Devices, Semiconductor Electronic Devices, and Neural Networks and Applications. Significant advances were made in all three areas. Under Quantum Electronic Devices considerable progress was made in overcoming the difficulties of realizing surface emitting optoelectronic devices. The novel growth technique of phase-locked epitaxy was developed which allowed for the improvement in control of layer thicknesses and improved performance of lasers. Under Semiconductor Electronic Devices, success was achieved in the deep sub-micron MOSFET program. Careful analysis of the fundamental issues that limit the continuation of the miniaturization of transistors has been an ongoing activity in this program. In the Neural Network and Applications Area, a prominent feature of the program has been the integration between theory and hardware. Revolutionary new architectures and algorithms for neural networks were investigated and tested on real-world applications, with particular attention given to applications of specific DOD interest.		
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## **DIRECTOR'S OVERVIEW**

Over the period June 6, 1990 to June 5, 1993, the Joint Services Electronics Program (JSEP) has supported 15 faculty investigators, 46 students, and produced 88 publications in journals or conference proceedings, 14 Ph.D. degrees and 22 M.S. degrees.

The research has been organized into three themes: Quantum Electronic Devices, Semiconductor Electronic Devices, and Neural Networks and Applications. Significant advances were made in all three areas during the contract period.

Under Quantum Electronic Devices, the difficulties of realizing surface emitting optoelectronic devices are now being overcome. The novel growth technique of phase-locked epitaxy was developed, allowing ultra-precise control of layer thicknesses, and was used to fabricate vertical cavity surface emitting lasers, which produced up to 10 mW output -- the highest power reported for such lasers. A surface emitting second-harmonic generator was invented and shown to achieve a 100-fold improvement in second harmonic conversion efficiency by using asymmetric quantum wells for phase matching.

Under Semiconductor Electronic Devices, spectacular success has been achieved in the deep sub-micron MOSFET program. Careful analysis of the fundamental issues that limit the continuation of the miniaturization of transistors has been an ongoing activity. One issue is that as transistor dimensions shrink, the number of dopants and interface traps within the active area of the device becomes so small that statistical fluctuations in the random distribution of these can begin to have a measurable effect on device behavior. In an effort to investigate this issue, single interface traps in PMOSFETs were observed and characterized for the first time via the fluctuations in current through a  $0.1 \mu\text{m} \times 0.3 \mu\text{m}$  transistor due to the filling and emptying of individual interface traps. An investigation of scalable device structures led to the identification of the SOI (silicon on insulator) device as the best opportunity for achieving functional devices below the  $0.1 \mu\text{m}$  barrier. A determined effort at understanding and overcoming the challenges involved in designing and fabricating such devices at this unprecedented dimension culminated in the realization and characterization of silicon MOSFETs with a world record switching speed of only 12 psec. In spite of considerable effort in this area world-wide, the Berkeley record still stands as the fastest of any silicon technology, including advanced SiGe heterojunction bipolar.

In the Neural Network and Applications Area, a prominent feature of our program has been the integration between theory and hardware. We have investigated revolutionary new architectures and algorithms for neural networks, and tested them on real-world applications, with some particular attention given to applications of specific DoD interest. One new architecture is the cellular neural network (CNN). This is a deceptively simple concept, with rather complex theoretical ramifications. Its close analogy to the structure of the visual cortex has proven to be of great advantage in pattern recognition problems. Another architecture developed for signal processing-type applications involves a Wigner-Ville transform time-frequency technique. This scheme was investigated for classifying sonar returns from different objects at different angles of observations and achieved a 95% success rate, outperforming all other known classification algorithms.

This has been a period of great accomplishment and excitement in the JSEP program at Berkeley. We look forward to a continued productive relationship with JSEP.

**LISTING OF PRINCIPAL INVESTIGATORS**

Nathan Cheung  
Leon Chua  
T. Kenneth Gustafson  
Chenming Hu  
Ping Ko  
Kam Lau  
M. Lieberman  
William Oldham  
Abhiram Ranade  
Alberto Sangiovanni-Vincentelli  
Carlo Sequin  
J. Stephen Smith  
Shyh Wang  
Eugene Wong  
Avideh Zakhor

STUDENTS PARTIALLY OR FULLY SUPPORTED BY JSEP: DEGREES AWARDED

Student	Degree	Year
Boothe, Bob	Ph.D.	93
Chan, James	M.S.	93
Chinnungrueng, Chedsada	Ph.D.	93
Chung, James	Ph.D.	90
Crounse, Kenneth	M.S.	91
Cruz-Moreno, Jose	M.S.	92
de Veciana, Gustavo	M.S.	90
Fong, Y.K.	Ph.D.	90
George, Peter	Ph.D.	90
Harshman, Patrick	M.S.	90
Hu, Limin	Ph.D.	90
Hung, Lawrence	M.S.	92
Kiang, Meng-Hsiung	M.S.	92
King, Chi-Chieh	M.S.	91
Lee, Angela	M.S.	91
Liang, Chunlin	Ph.D.	90
Liang, Guo Chun	Ph.D.	90
Lin, Hong	Ph.D.	92
Moon, J.E.	Ph.D.	90
Noriego-Asturias, Jorge	M.S.	92
Raghunath, M.T.	Ph.D.	93
Sin, C.K.	M.S.	90
Walker, Jeffrey	M.S.	90
Wann, Hsing-jen	M.S.	92
Wilson, Gordon	M.S.	90

11 Ph.D.'s and 14 M.S.'s

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R.D. Clay and C.H. Séquin, "Limiting Fault-Induced Output Errors in ANN's," submitted to International Joint Conference on Neural Networks, Seattle, Washington, July 1991.

G. de Veciana and A. Zakhor, "Neural Net Based Continuous Phase Modulation Receivers," submitted for publication to *IEEE Transactions on Communications*.

S.P. Dijaili, A. Dienes, and J.S. Smith, "ABCD Matrices for Dispersive Pulse Propagation," *IEEE Journal of Quantum Electronics*, Vol. 26, No. 6, pp. 1158-1164, June 1990.

S.P. Dijaili, J.M. Wiesenfeld, G. Raybon, C.A. Burtus, A. Dienes, J.S. Smith, J.R. Whinnery, "Cross Phase Modulation in a Semiconductor Laser Amplifier Determined by a Dispersive Technique," submitted to *Applied Physics Letters*.

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H. Lin and J.S. Smith, "Optical Time-Division Demultiplexing Using Second-Order-Optical Nonlinear Effects," *Appl. Phys. Lett.*, 59 (22), November 1991.

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Z.H. Liu, J.H. Huang, J. Duster, P.K. Ko, C. Hu, M.C. Jeng, and Y.C. Cheng, "Threshold Voltage Modeling for Deep-Submicrometer Conventional LDD MOSFETs at 300K and 85K," *Proceedings of 1991 International Semiconductor Device Research Symposium*, Charlottesville, Virginia, December 4-6, 1991, pp. 411-414.

R. Moazzami, N. Akt, Y. Nissan-Cohen, W.H. Sphepherd, M.P. Brassington, and C. Hu, "Impact of Polarization Relaxation on Ferroelectric Memory Performance," *1991 Symposium on VLSI Technology Digest of Technical Papers*, pp. 61-62, Oiso, Japan, May 1991.

J.E. Moon, C. Galewski, M. Wong, W.G. Oldham, P.K. Ko, and C. Hu, "A Deep-Submicrometer Elevated Source/Drain LDD Structure Fabricated Using Hot-Wall Epitaxy," *Proceedings*

*Technical Papers, 1991 International Symposium on VLSI Technology, Systems, and Applications, Taipei, Taiwan, May 1991, pp. 117-121.*

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A.L. Oliveira and A. Sangiovanni-Vincentelli, "Synthesis of Minimal Multi-Level Networks," to be presented at *Neural Networks for Computing Workshop*, Snowbird, Utah, April 1992.

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C-K. Sin, A. Kramer, V. Hu, R. Chu and P.K. Ko, "EEPROM as an Analog Storage Device with Particular Applications in Neural Networks," *1992 IEEE Transactions on Electron Devices*, accepted for publication in June 1992 issue.

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## PUBLICATIONS/PAPERS/PRESENTATIONS

March 1992 - June 1993

F. Assaderaghi, J. Chen, P.K. Ko and C. Hu, "Measurement of Electron and Hole Saturation Velocities in Silicon Inversion Layers Using SOI MOSFETs, *"Proceedings of the IEEE SOI Conference*, p. 112, Oct. 1992.

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J. Chan, "Investigation of AlN as an Insulated-Gate and Wide Bandgap Semiconductor Material," M.S. Thesis, University of California, Berkeley, 1993.

C. Chinrungrueng, "Evaluation of Heterogeneous Architectures for Artificial Neural Networks," Ph.D. Thesis, University of California, Berkeley, April 1993.

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K. Crounse, "Image Halftoning Using Cellular Neural Networks," Master's Thesis, University of California, Berkeley, December 1991.

J. Cruz-Moreno, "A Cellular Neural Network Chip," Master's Thesis, University of California, Berkeley, December 1992.

G. de Veciana, "Neural Net Based Continuous Phase Modulation Receivers," Master's Thesis, University of California, Berkeley, October 1990.

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M. Kiang, "Utilizing Plasma Immersion Ion Implantation and Electroless Plating for Planarized Copper Metalization," Master's Thesis, University of California, Berkeley, May 1992.

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